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(71) Applicant: EASTMAN KODAK COMPANY (a New Jersey corporation)
343 State Street
Rochester New York 14650(US)

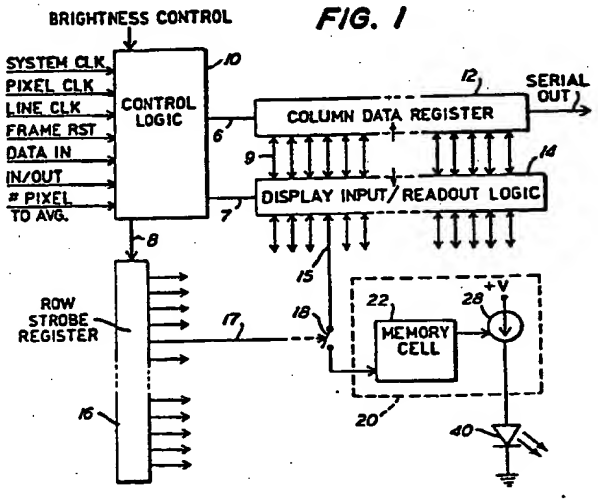
(72) Inventor: Bell, Cynthia Sue Eastman Kodak Company
Patent Department 343 State Street
Rochester New York 14650(US)
Inventor: Gaboury, Michael Joseph Eastman Kodak Company
Patent Department 343 State Street
Rochester New York 14650(US)

(74) Representative: Parent, Yves et al
Kodak-Pathé Département Brevets et Licences Centre de Recherches et de Technologie Zone Industrielle
F-71102 Chalon-sur-Saône Cédex(FR)

(54) Electroluminescent storage display with improved intensity driver circuits.

(57) In the present invention a matrix array of organic electroluminescent storage display elements along with row and column selection circuitry (12, 14, 16) are used to select the particular display elements (40) within the matrix to be illuminated. Interposed between the column and row selection electronics are a plurality of memory cells (22) receiving as inputs bit values (B_n-B_o) that correspond to the desired intensity requested from a display element (40). The memory cells (22) output activation signals which drive corresponding MOS switches (24) each of which in turn is parallel connected as part of a current driver source (28) feeding a single display element (40). Activation of one or more of the MOS switches (24) provides a controlled amount of current to be applied to the display element (40) to in turn provide a related amount of light from the display element (40).

FIG. 1



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ELECTROLUMINESCENT STORAGE DISPLAY WITH IMPROVED INTENSITY DRIVER CIRCUITS

The present invention relates to the field of thin film electroluminescent display devices and, more particularly, to organic electroluminescent display devices with driver circuitry.

Electroluminescence is the emission of a light from a luminescent material when an electrical field of proper value is applied to the material. This property has been utilized in the prior art to construct display panels. The first wave of devices were of the AC type which used the luminescent material as the dielectric in a parallel plate capacitor where one of the parallel plates was transparent. When an alternating voltage was applied to the parallel plates the luminescent material emitted light. By depositing rows of conductive material on one surface of the luminescent material and columns of conductive material on the opposite surface, an X-Y matrix is formed. At each crossover point of a column and a row a pixel for a video display is formed. With the proper excitation at the crossover points the pixel positioned at that point will emit light. Drive circuits are then coupled to the rows and the columns to vary the level of current or voltage that is applied as a function of the amount of light that is to be generated by each pixel.

Advances in the electroluminescent material art have led to organic materials being used in such type displays which materials provide high brightness levels, and low DC voltage requirements along with multicolors. In addition, recent developments have resulted in display panels with a high density of addressable pixels. With such displays, it is desirable to be able to store imaging data so that the display can be operated without external memory and without continual refreshing. In addition, it would be advantageous to be able to control the brightness of the display with binary signals rather than analog signals thereby permitting the display to be driven by a computer.

According to one aspect of the present invention, each organic electroluminescent pixel element in a matrix of organic electroluminescent pixel elements is provided with a plurality of memory cells for receiving a corresponding plurality of binary input bits. The output of each memory cell is connected to a current driver such that each memory cell controls a portion of the total current applied to the pixel element. Each memory cell activates a MOS transistor to place it into parallel circuit with other activated MOS transistors such that the combination of parallel activated transistors controls the current flowing to the pixel element and in turn the intensity of the light generated by the pixel element. The memory driver circuit for each pixel element thus acts as a memory cell, a D/A converter, and as an electronic switch for controlling the current supplied to the pixel element. This particular driver configuration allows for a continuous, static current to be driven through the pixel element for each brightness level in response to a binary number. In turn, this reduces the peak drive current required to light the pixel elements and indirectly reduces the voltage and the power consumption levels for a matrix display incorporating the improved intensity drivers.

Figure 1 is a block diagram illustrating the arrangement of an addressable matrix display incorporating the improved driver circuits.

Figure 2 is a block circuit diagram of an improved driver circuit of the type used in Figure 1.

Figure 3 is a transistor level schematic of a memory cell that may be used as a memory cell of Figure 2.

Figure 4 is a transistor level schematic of a memory cell which also may be used as a memory cell of Figure 2.

Figure 5 is a drawing of the layers of one type of electroluminescent device that can be used as the pixel element in a matrix of such elements.

In Figure 1, a control logic circuit 10 receives incoming data (DATA IN) and other interface timing signals. The control logic synchronizes the incoming data with the signals PIXEL CLK, LINE CLK, and FRAME RST as is standard procedure. A SYSTEM CLK signal provides a high speed clock for controller internal timing. An IN/OUT line allows data to be read in and out of the memory storage. This mode is also useful in automating the testing of the display circuitry. The #PIXEL TO AVG. signal allows data from sources of varying resolution to be displayed. Normally, the data would be subsampled or otherwise pre-processed external to the display system. This feature allows the data to be averaged while it is incoming direct from the data source. A BRIGHTNESS CONTROL allows for an adjustment of the display brightness level for various applications. The level of this input may be controlled, for example, by a user through a potentiometer, by a light meter circuit, or by other means.

Outputs from the control logic circuitry are directed to a column data register 12, a display input/readout logic circuit, and a row strobe register 16 over lines 6, 7, and 8, respectively. The parallel outputs 9 from the column data register 12 are connected to the display input/readout logic 14 to provide bidirectional data paths therebetween. The display input/readout logic 14 has a corresponding number of bidirectional lines output 15.

The row strobe register 16 has a number of output lines 17 corresponding in number to the number of rows in a driven display matrix.

A memory driver circuit 20 is connected to a column line 15 by means of a MOS switch 18 when the row line 17 associated with a memory driver circuit is selected (energized). The output of the memory driver circuit 20 is connected to an electroluminescent cell 40 (pixel element).

An image display is formed by physically positioning a plurality of these pixel elements 40 closely together, generally in a matrix configuration of rows and columns or by forming the pixel elements 40 in a VLSI multilayer type structure.

Each pixel element is provided with its own memory driver circuit 20. Within each memory driver circuit there is a memory cell 22 that is connected on its input via the switch 18 to the line 15. The output of the memory cell is connected to a current drive source 28. The current driver source is powered by a voltage supply +V to provide a driving current to the pixel element 40. The magnitude of the driving current is controlled by the output signal from the memory cell 22 which magnitude in turn determines the brightness level of the light emitted by the pixel element 40.

The combination of an active IN signal and FRAME RST signal causes the controller 10 to load in new data for display. This is accomplished by setting the display input/readout 14 to its read-in state with an enable signal on line 7. The incoming data is averaged as directed by the #PIXEL TO AVG. signal, and then passed on to the memory driver circuitry 20. This is done by conveying the data serially to the column data register 12 over line 6 in a line-by-line fashion. When an entire line has been conveyed, the control logic sends out a pulse to the row strobe register 16 over line 8, which closes the transistor switch(s) 18 associated with that row, thereby enabling the transfer of column data to the memory cell(s) 22. Following the loading of the data, the row switch(s) 18 are reopened and the next line is loaded.

The combination of an active OUT signal and FRAME RST signal cause the control logic to set the display input/readout 14 to its read-out state. As each row strobe line 17 is enabled, and the logical state of each memory cell 22 is sensed on each column line 15, the data in each memory cell is transferred in parallel to the column data register 12 which serially conveys the data out, line-by-line on the serial out line.

In Figure 2 a group of memory cells, 22n through 22n-3, responding to binary bit signals, B_n through B_{n-3} activate one or more MOS transistors 24. The MOS transistors 24, 26, and 27 form the current driver 28 for driving the pixel element 40. The MOS transistors 26 and 27 are connected and sized to function as current mirrors, that is, the current through MOS transistor 27, which can be called I_{pixel}, is equal to the current flowing through MOS transistor 26, which current can be called I_2. The current I_2 is a function of the number of MOS transistor 24 that are turned ON or OFF (actively connected in parallel). With all MOS transistors 24 turned ON the highest level of current flows through the pixel element 40. With all of the MOS transistors 24 in an OFF state the pixel element 40 is not illuminated.

Generally speaking, when devices 26 and 27 are the same size the following relationship holds true: $I_{pixel} = I_2 + I_n + I_{n+1} + \bullet\bullet\bullet\bullet$. If each MOS transistor is fabricated to have a different current flow when it is ON then a selection can be made as to which transistors are turned ON, in combination, to achieve the desired intensity level.

Selection of the MOS transistors 24 is accomplished by applying an enable signal to the ROW inputs of the memory cells 22n through 22n-3. The column bits are applied to the B_n inputs prior to the ROW enable signal and are latched into the memory cells upon receipt of the ROW enable signal.

Figure 3 illustrates a first circuit implementation for a memory cell 22_n. A column input, signal B_n, is gated to the input of a CMOS inverter gate 36 and to one electrode of a MOS transmission gate 34 via a MOS transmission gate 30. A ROW input is connected to the input of a CMOS inverter 32, to the gate electrode of the MOS transistor 34, and to the gate electrode of the MOS transistor 30. One electrode of the MOS transistor 34 is connected to the input to a CMOS inverter 38. The output of the memory cell 22_n directed to the gate electrode of an associated MOS transistor 24.

Figure 4 illustrates a second circuit implementation for a memory cell 22_n. A MOS transistor 31 has its drain electrode connected to receive the signal B_n, its gate electrode is connected to receive the ROW signal and its source electrode is connected to the inputs of CMOS inverters 33 and 35. The outputs from inverter 33 and inverter 35 are connected to the gate electrode of an associated MOS transistor 24.

Referring to Figure 5, the pixel element 40 is formed on a glass base 41 having an indium-tin-oxide (ITO) layer 42 vacuum deposited thereon. A positive electrode is affixed to layer 42. A first organic layer 43 of an aromatic diamine is vacuum deposited on layer 42.

A second organic layer 44 is a luminescent ALq_3 film which is vacuum deposited onto layer 43. An electrode 45, which is an alloy or mixture of magnesium and silver (MgAg), is vacuum deposited onto layer 44. A conductor is connected to layer 45 and to a source of negative potential, with

respect to the positive potential of layer 42. The device thus formed is an organic electroluminescent diode which is responsive to d.c. to provide a light output. Such a device is described in detail in an article entitled "Organic Electroluminescent Diodes" by C.W. Tang, Appl. Phys. Lett. 51(12), 21 September 1987, pps 913 and 914.

To form a large scale display a plurality of these elements can be positioned together in a frame type structure or they may be fabricated as either a single or as separate VLSI chips which are interconnected to form the display.

Claims

1. An electroluminescent storage display with improved intensity driver circuits characterized by:
an electroluminescent element (40);
a plurality of memory elements (22);
a current source (28) connected in circuit to said electroluminescent element (40);
a plurality of elements (24), corresponding in number to said plurality of memory elements (22), each connected to a respective memory element (22) and responsive to the signals stored therein for causing an incremental current to flow from said current source (28) to said electroluminescent element (40); and
means (10, 12, 14, 16, 18) for applying signals (B_n-B_o) to said memory elements (22) indicative of the intensity desired from said electroluminescent element (40).

2. The electroluminescent storage display of claim 1 wherein said plurality of elements (24) are MOS transistors each having a gate electrode connected to a respective memory element (40).

3. The electroluminescent storage display of claim 1 wherein said means for applying signals to said memory elements is comprised of: a plurality of binary bits (B_n-B_o) corresponding in number to said plurality of memory elements (40) and an enabling signal source for providing an enabling signal (16) for loading said binary bits (B_n-B_o) into said memory elements (40).

4. An electroluminescent storage display with improved intensity driver circuits characterized by;
a column data register means (12) having an input (6) for serially receiving image signals, and having a plurality of parallel outputs (9) for providing said image signals thereon;
an input/output logic means (14) responsive to an enable signal (7), and coupled to the plurality of parallel outputs (9) of said column data register means (12) for gating said image signals to respective column outputs (9);
a row strobe register means (16) responsive to an input signal (8) for sequentially providing an enabling strobe signal on each of a plurality of row outputs (17);
a plurality of switch means (18), each connected to a respective one of a plurality of row outputs (17) of said row strobe register means (16) for connecting a respective one of said column outputs (15) of said input/output logic means (14) to a switch output;
a plurality of memory driver circuit means (20) having an input connected to the switch output of a respective switch means (18) and having an output for providing a current as a function of the image signal received on its input; and
a plurality of electroluminescent display means (40) each connected to an output of a respective memory driver circuit means (20) for illumination by the provided current therefrom.

5. An electroluminescent storage display according to claim 4 and further comprising:
a control logic means (10) responsive to input control signals, image data signals and brightness signals for providing image signals to said column data register (12), enable signals (7) to said input/output logic means (14), and an input signal (8) to said row strobe register means (16).

6. An electroluminescent storage display according to claim 4 wherein each of said plurality of memory driver circuit means (20) is comprised of:
a plurality of memory elements (22);
a current source (28) connected in circuit to an electroluminescent display means (40);
a plurality of elements (24) corresponding in number to said plurality of memory element (22), each connected to a respective memory element (22) and responsive to the signals (B_n-B_o) stored therein for causing an incremental current to flow from said current source (28) to said electroluminescent display means (40); and additionally
means (16, 12, 14) for applying signals to said memory elements (22) indicative of the intensity desired from said electroluminescent display means.

7. The electroluminescent storage display of claim 6 wherein said plurality of elements (24) are MOS transistors each having a gate electrode connected to a respective memory element (22).

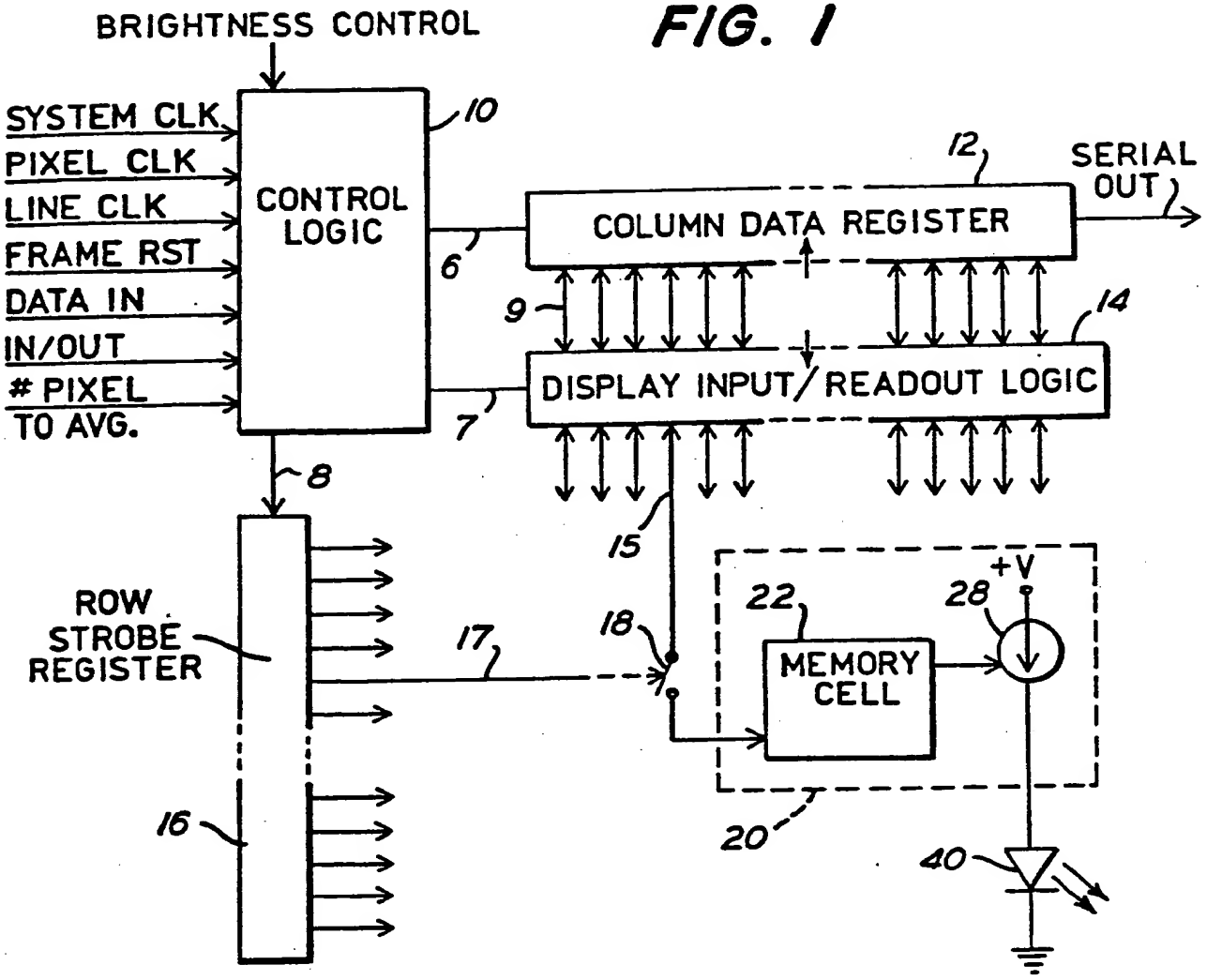
8. The electroluminescent storage display of claim 6 wherein said means for applying signals to said memory elements is comprised of:
a plurality of binary bits (B_n-B_o) corresponding in number to said plurality of memory elements (22) and an enabling signal source (16) for providing an enabling signal (ROW) for loading said binary bits (B_n-B_o) into said memory elements (40).

9. an electroluminescent display matrix characterized by:
a plurality of electroluminescent elements (40) arranged in a display;

a plurality of storage means (22) for each of said plurality of electroluminescent elements (40) for receiving binary number signals (B_n-B_o) corresponding to the intensity level desired from an associated electroluminescent element (40);
a plurality of current sources (28) each coupled to a respective plurality of said storage means (22) and an associated electroluminescent element (40) for providing a current as a function of the binary number signals (B_n-B_o) stored in said storage means (22).

10. The electroluminescent display matrix according to claim 9 wherein each of said plurality of current sources (28) is comprised of:
a two MOS device current mirror (26, 27), with the first of said MOS devices (27) connecting said electroluminescent element (40) to a source of power (+V) and with the second of said MOS devices (26) connecting said source of power to a selectable current means (24); and
a selectable current means (24) connected to said plurality of storage means (22) and responsive to the signals stored therein for causing the current in said second MOS device (26) to be a function of the signals (B_n-B_o) stored in said plurality of storage means (22).

FIG. 1



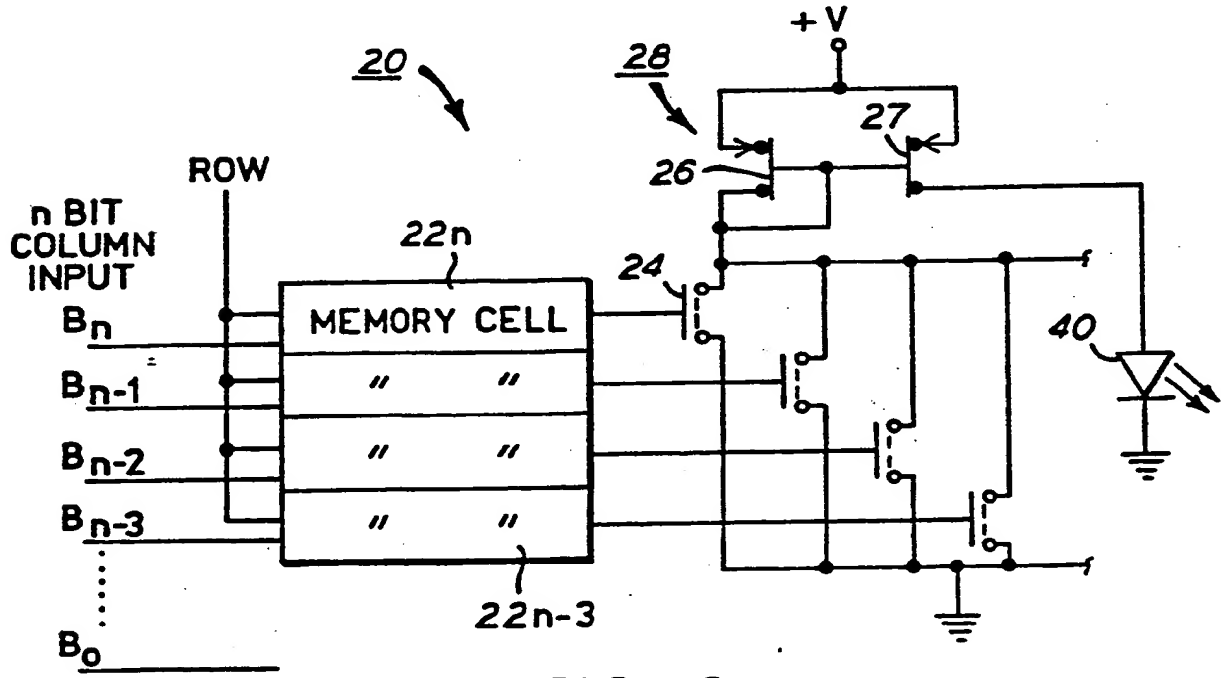


FIG. 2

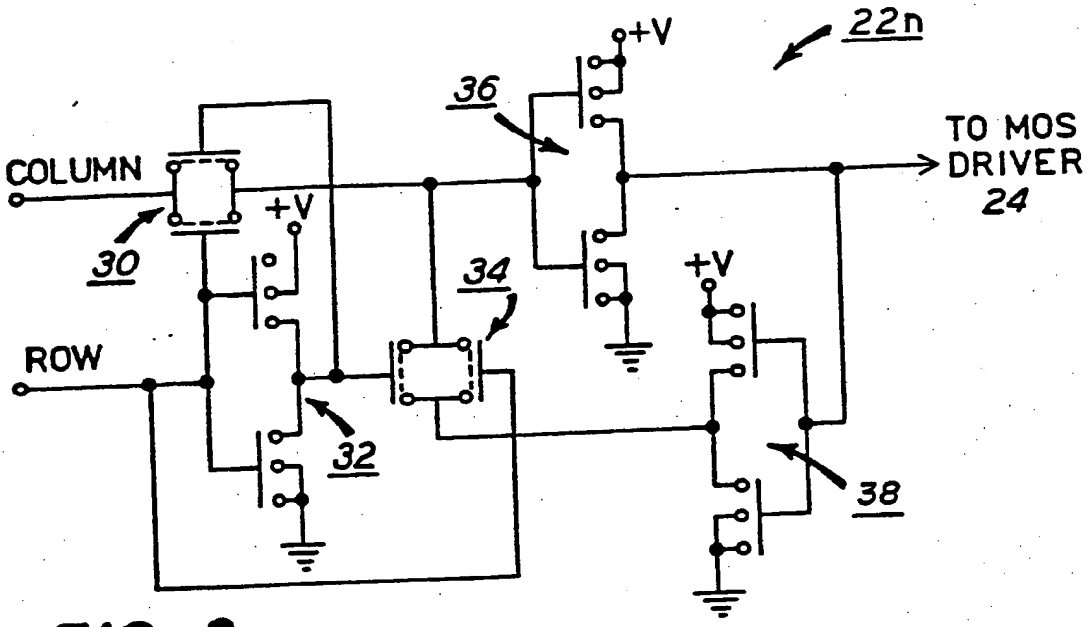


FIG. 3

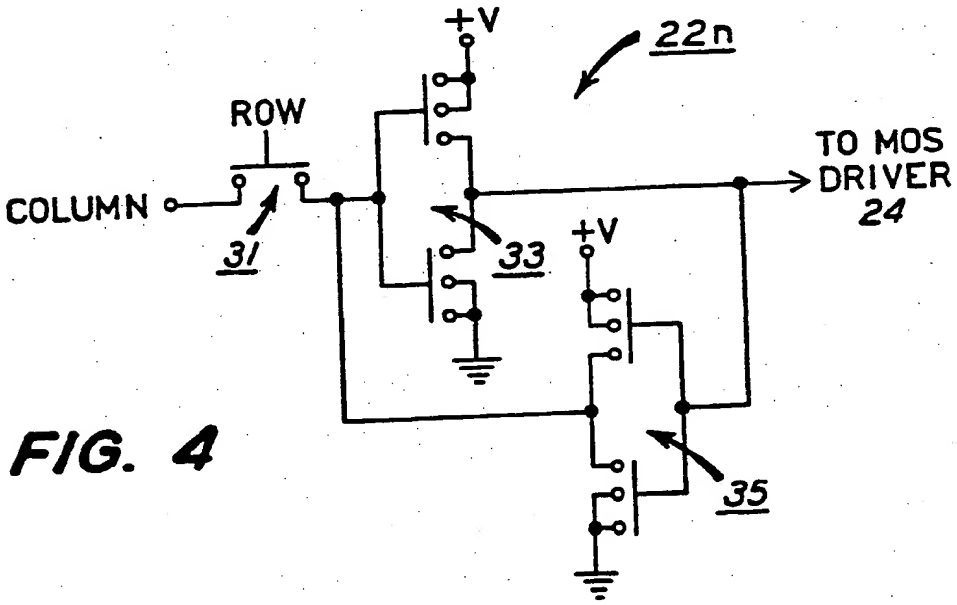
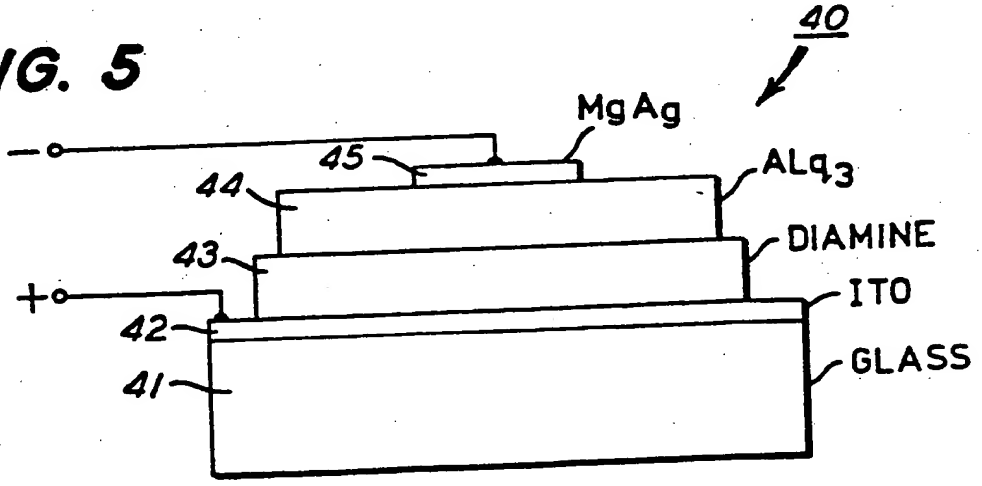


FIG. 4

FIG. 5



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(71) Applicant: EASTMAN KODAK COMPANY (a New Jersey corporation)
343 State Street
Rochester New York 14650(US)

(72) Inventor: Bell, Cynthia Sue Eastman Kodak Company
Patent Department 343 State Street
Rochester New York 14650(US)
Inventor: Gaboury, Michael Joseph Eastman Kodak Company
Patent Department 343 State Street
Rochester New York 14650(US)

(74) Representative: Parent, Yves et al
Kodak-Pathé Département Brevets et Licences Centre de Recherches et de Technologie Zone Industrielle
F-71102 Chalon-sur-Saône Cédex(FR)

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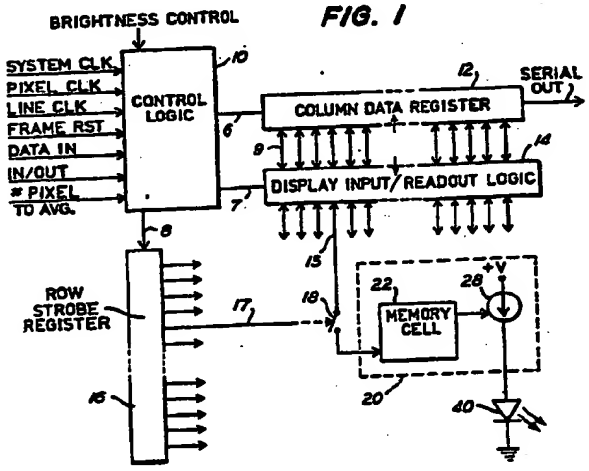
FIG. 1



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EUROPEAN SEARCH REPORT

Application Number

EP 89 42 0391

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.5)
A	US-A-3 740 570 (G.R. KAELIN et al.) * the entire document *	1,4,5,9	G 09 G 3/32
A	US-A-3 629 653 (M. IRWIN) * the entire document *	1,4,5,9	
A	US-A-4 559 535 (R.W. WATKINS et al.) * column 7, line 41 - column 10, line 66; figures 6-10 *	1,4,5,9	

TECHNICAL FIELDS SEARCHED (Int. Cl.5)

G 09 G
H 04 N
H 05 B

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
BERLIN	01-03-1990	KELPERIS K.

CATEGORY OF CITED DOCUMENTS

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